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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/720,958	11/24/2003	Arun Ramakrishnan	03-1098/L13.12-0252	5206

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EXAMINER	
RAO, SHRINIVAS H	

ART UNIT	PAPER NUMBER
2814	

DATE MAILED: 11/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/720,958	RAMAKRISHNAN ET AL.	
	Examiner	Art Unit	
	Steven H. Rao	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *24 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *3/31/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

The Application as currently filed does not claim priority from any previously filed patent application. Therefore currently the earliest available filing date is the U.S.> filing date namely November 24, 2003.

Information Disclosure Statement

Acknowledgment is made of receipt of Applicant's Information Disclosure Statement (PTO-1449) filled March 01, 2004.

The references on PTO 1499 submitted on 03/01/2004 are acknowledged. All the cited references have been considered. However the foreign patents and documents cited by applicant are considered to the extent that could be understood from the abstract and drawings.

Drawings

New corrected drawings in compliance with 37 CFR 1.121(d) are required in this application because the three sheets of drawings filed on March 01, 2004 include several informalities, namely figure1 has a extra bracket on Left hand side without a reference numeral . All three sheets include information regarding Applicants', phone number Attorney Docket number , etc. that should be deleted from the front sheet of the drawings.

Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1- 32rejected under 35 U.S.C. 102(e) as being anticipated by Hosomi (U.S. Printed Patent Application Publication No. 2003/0209807 published on November 13, 2003 , now U.S. Patent No. 6,768,206, herein after Hosomi).

(Paper copies of cited U.S. patents and U.S. patent application publications will ceased to be mailed to applicants with Office Actions as of June 2004. Paper copies of foreign patents and non-patent literature will continue to be included with Office Actions. These cited U.S. patents and patent application publications are available for download

via the Office's PAIR. As an alternate source, all U.S. patents and patent application publications are available on the USPTO web site (www.uspto.gov), or ((http://portal.uspto.gov/external/portal/pair) from the Office of Public Records and from commercial sources. Applicants' are referred to the Electronic Business Center (EBC) at http://www.uspto.gov/ebc/index.html or 1-866-217-9197 for information on this policy. Requests to restart a period for response due to a missing U.S. patent or patent application publications will not be granted).

With respect to claim 1 Hosomi describes a flip chip substrate comprising: plurality of conductive layers, (Hosomi para 0005lines 3-5) including a top layer (Hosomi para 0005 line 1) and a bottom layer; (Hosomi para 005 line 1) a first plurality of contacts, including first and second contacts corresponding a differential signal pair, (Hosomi para 0002 # 16) which are arranged on the top layer within a die bonding area; (Hosomi para 0002 lines 3-7) second plurality of contacts, including third and fourth contacts corresponding to the differential signal pair, which are arranged on the bottom layer; (Hosomi para 0002 lines 3-7) and first and second traces routed between the first and third contacts and between the second and fourth contacts, respectively, (Hosomi para 0006 lines 1-4) wherein the second trace routed the die bonding area on different one of the layers than the first trace and comprises via the die bonding area extending from the top layer another of plurality of layers, (Hosomi figure 8 , para 0015 lines 1-5) wherein the via is laterally offset from the second contact direction toward the first contact. (Hosomi figures 8-10, paras 0031 and 0032).

With respect to claim 2 Hosomi describes the flip chip substrate of claim 1 wherein: the first trace is routed outwardly from the first contact toward an edge the die bonding area along the top layer; and the second trace is routed from the second contact to the different layer and outwardly toward the edge die bonding area along the different layer. (Hosomi figure 9 # 146, para 033 lines 6-7).

With respect to claims 3 and 25 Hosomi describes the flip chip substrate of claim 2 wherein the edge of the die bonding area is a nearest edge of the die bonding area to the first and second contacts. (Hosomi figure 9)

With respect to claims 4 and 26 Hosomi describes the flip chip substrate of claim 2 wherein the different layer comprises the bottom layer, which non-adjacent to the top layer. (Hosomi para 002, figures 1-9, etc.).

With respect to claims 5 and 27 Hosomi describes the flip chip substrate of claim wherein different layer is disposed between the top layer and the bottom layer. (Hosomi para 0005 lines 3-5)

With respect to claims 6 and 28 Hosomi describes the flip chip substrate of claim wherein the different layer is immediately adjacent to the top layer. (Hosomi para 0005 lines 3-5)

With respect to claims 7 and 29 Hosomi describes the flip chip substrate of claim 2 wherein: the second trace is routed from the different layer back up the top layer externally to the die bonding area; and the first and second traces extend along the top layer outside of the die bonding area respective vias located externally the die bonding

area and are routed downwardly from the respective vias toward the third and fourth contacts, respectively. (Hosomi para 0006 lines 9-16)

With respect to claims 8 and 30 Hosomi describes the flip chip substrate claim wherein the respective vias are located in a region on the top layer that generally vertical of the third and fourth contacts. (Hosomi para 006 line 16-25).

With respect to claim 9 and 31 Hosomi describes the flip chip substrate claim wherein the first and second contacts form a pair of adjacent signal contacts in the die bonding area. (Hosomi para 009 lines 3-5).

With respect to claim 10 Hosomi describes the flip chip substrate claim wherein the third and fourth contacts form pair of adjacent signal contacts on the bottom layer, external the die bonding area.(Hosomi figure 6 para 0006 lines 1-3 and 0009 line 9-10).

With respect to claim 11 and 32 Hosomi describes the flip chip substrate of claim wherein the second contact is located further from a nearest edge of the die bonding region than the first contact. (Hosomi para 0009 lines 5-6)

With respect to claim 12 Hosomi describes the flip chip substrate of claim 1 wherein: the third and fourth contacts are adjacent to one another on the bottom layer; and the first and second traces comprise respective vias extending from the bottom layer to another of the plurality of layers, wherein the respective vias are laterally offset toward one another relative to centers of the third respectively. and fourth contacts, (Hosomi para 006, 009 and 0011).

With respect to claim 13 Hosomi describes a flip chip substrate comprising:

a plurality of conductive layers, including a top layer and a bottom layer; a first plurality of contacts, including first and second contacts corresponding to a differential signal pair, which are arranged on the top layer within a die bonding area; a second plurality of contacts, including third and fourth contacts corresponding the differential signal pair, which are arranged on the bottom layer; a first trace electrically connecting the first and third contacts having first segment extending outwardly from the first contact toward an edge of the die bonding area along the top layer; and second trace electrically connecting the second and fourth contacts, wherein the second trace extends from the second contact to second one layers within the die bonding area, which located between the top and bottom layers, extends outwardly from the die bonding area along the second layer, and returns the top layer externally to the die bonding area, and wherein the first and second traces extend along the top layer outside of the die bonding area to respective vias and extend downwardly from the respective vias toward the third and fourth contacts, respectively. (rejected for reasons set out under claims 1-12 above).

With respect to claim 14, Hosomi describes the flip chip substrate of claim 13 wherein the second trace comprises a further extending from the top layer to the second layer within the die bonding area and wherein the further via is laterally offset from a center of the second contact in a direction toward the first contact. (Hosomi paras 006, 009 and 0011).

With respect to claim 15 Hosomi describes the flip chip substrate of claim 13 wherein the first and second traces are routed outwardly along the top and second

layers, respectively, toward a nearest edge of the die bonding area to the first and second contacts. (Hosomi figures).

With respect to claim 16 Hosomi describes the flip chip substrate of claim 13 wherein the second layer immediately adjacent the top layer. (Hosomi figures paras 0004-0006).

With respect to claim 17 Hosomi describes the flip chip substrate of claim 13 wherein the respective vias are located adjacent to one another in region on the top layer that is generally vertical of the third and fourth contacts. (Hosomi figures para 0011).

With respect to claims 18 and 19 Hosomi describes the flip chip substrate of claim 13 wherein the first and second contacts form a pair of adjacent signal contacts and the third and fourth contacts form a pair of adjacent signal contacts in the die bonding area. (Hosomi para 009 lines 3-5).

With respect to claim 20 Hosomi describes the flip chip substrate of claim 13 wherein the second contact is located further from a nearest edge of the die bonding region than the first contact. (Hosomi para 009 lines 3-5).

With respect to claim 21 Hosomi describes the flip chip substrate of claim 13 wherein: the third and fourth contacts are adjacent one another on the bottom layer; and the first and second traces comprise second pair respective vias extending from bottom layer to another of the plurality of layers, wherein the second pair respective vias are laterally offset toward one another relative centers of the third and fourth contacts, respectively. (rejected for reasons set out under claims 13-20 above).

With respect to claim 22 Hosomi describes a flip chip substrate comprising: a plurality of conductive layers, including a top layer and a bottom layer; a first plurality of contacts, including first and second contacts corresponding to a differential signal pair, which are arranged on the top layer within a die bonding area; a second plurality of contacts, including third and fourth adjacent contacts corresponding to the differential signal pair, which are arranged on the bottom layer; and first and second traces routed between the first and third contacts and between the second and fourth contacts, respectively, first and second traces comprising pair of respective vias extending from the bottom layer to another of the plurality of layers, wherein the pair of respective vias are laterally offset toward one another relative to centers of the third and fourth contacts, respectively. (rejected for reasons set out under claims 1-21 above).

With respect to claim 23 Hosomi describes the flip chip substrate of claim 22 wherein: the second trace is routed of the die bonding area on different one layers than the first trace and comprises a via the bonding area extending from the top layer another of the plurality of layers, and wherein the via laterally offset from the second contact in a direction toward the first contact. (Hosomi figures).

With respect to claim 24 Hosomi describes the flip chip substrate of claim 23 wherein: the first trace routed outwardly from the first contact toward an edge of the die bonding area along the top layer; and the second trace is routed from the second contact to the different layer and outwardly toward the edge of the die bonding area along the different layer. (Hosomi figures 6,9, paras 0013,0031,etc.).

Any inquiry concerning this communication or earlier communication from the examiner should be directed to Steven H. Rao whose telephone number is (571) 272-1718. The examiner can normally be reached on Monday- Friday from approximately 7:00 a.m. to 5:30 p.m.

Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 308-0956. The Group facsimile number is (703) 308-7724.

Steven H. Rao

Patent Examiner

Oct 27, 2004.

DOUGLAS WILLE
PRIMARY EXAMINER